



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,853	07/15/2003	Karen L. Noel	200308870-1	7585

22879 7590 12/31/2007  
HEWLETT PACKARD COMPANY  
P O BOX 272400, 3404 E. HARMONY ROAD  
INTELLECTUAL PROPERTY ADMINISTRATION  
FORT COLLINS, CO 80527-2400

EXAMINER
----------

PANTOLIANO JR, RICHARD

ART UNIT	PAPER NUMBER
----------	--------------

2194

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

12/31/2007

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM  
mkraft@hp.com  
ipa.mail@hp.com

# Office Action Summary

Application No.

10/619,853

Applicant(s)

NOEL ET AL.

Examiner

Richard Pantoliano Jr

Art Unit

2194

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 08 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMPSON  
SUPERVISORY PATENT EXAMINER

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Amendment***

1. This Office Action is filed in response to amendments filed for Application# **10/619,853** filed on **13 October 2006** and arguments submitted in appeal brief filed **08 October 2007**. **Claims 1-20** are currently pending and have been considered below.
2. In view of the appeal brief filed on **08 October 2007**, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1, 3, and 12-14** are rejected under 35 U.S.C. 102(b) as being anticipated by Dunn (Dunn, Joe; Shucker, Brian; and Browne, Rich. "The Design and Implementation of JaDiSM". University of Colorado at Boulder, December 2001).

5. As to **Claim 1**, Dunn teaches the invention substantially as claimed including the method comprising:

a) determining, by a first program (*pg. 3, source code example*), an attribute of a first functional unit by referencing a virtual memory address (*pg. 1, para. 3 and pg. 3, source code example*), the first functional unit comprising a first processor and a random access memory (RAM) coupled to the first processor in a computer system (*pg. 7, para. 4*), and the first program executing in the first functional unit (*The Java Distributed Shared Memory (JaDiSM) node software runs on each processor and memory. Since the Linux Operating System (OS) with virtual memory addressing enabled is used as the OS running on each of the nodes, all accesses to memory, including the accessing of the NodeID performed in the source code example, require referencing a virtual address*);

b) determining, by a second program, an attribute of a second functional unit by referencing the virtual memory address, the second functional unit comprising a second processor and a RAM coupled to the second processor in the computer system, and the second program executing in the second functional unit (*See above*); and

c) wherein the referencing the virtual memory address by the first program provides a pointer to an attribute stored in the RAM of the first functional unit and wherein the referencing the virtual memory address by the second program provides a pointer to an attribute stored in the RAM of the second functional unit and the pointer and attribute of the second functional unit are different than the pointer and attribute of the first functional unit *(Since accessing the NodeId requires accessing a local memory address, the particular processor/memory pair will have to obtain the real address (pointer) to the memory location containing the NodeId data. Since all of the node software executed is located on different processor/memory pairs but are otherwise identical, the virtual addresses that the programs use are the same, but the real addresses that they map to on each particular processor/memory pair would be unique to that pair, thereby meeting the claim limitation).*

6. As to **Claim 3**, Dunn further teaches wherein determining an attribute of the first functional unit further comprises determining a functional unit identification number (pg. 3, source code example) *(The retrieval of the "NodeId" meets this claim limitation).*

7. As to **Claim 4**, Dunn further teaches wherein determining an attribute of the first functional unit further comprises determining low and high physical address of the RAM of the first functional unit (pg. 1, para. 3; pg. 5, para. 3-6 and pg. 6, Figure 4) *(Linux, the operating system on which JaDiSM executes, inherently divides a system into high and low memory, placing executable code that is specific to the OS in low memory and*

Art Unit: 2194

*placing any user applications in high memory. Since the JaDiSM memory locations are being mapped to specific areas, the nodes must inherently be aware of the boundary to avoid allocating memory in a location to which it does not have access, thereby meeting the claim limitation).*

8. As to **Claim 12**, Dunn discloses the invention substantially as claimed including a computer readable medium containing an executable program that, when implemented, implements the method comprising:

a) reading a functional unit identifier from a random access memory (RAM) coupled to a program in which the program executes (*pg. 1, para. 3 and pg. 3, source code example*)(*The determination of the "NodeId" by the application meets this claim limitation*);

b) determining within the functional unit, identified by the functional unit number, the program is executing (*pg. 1, para. 3 and pg. 3, source code example*) (*The ability to determine the NodeId in the system is predicated on the basis that the program is already executing*; and

c) addressing data at a same virtual address by different processors in different functional units, wherein each processor in a different functional unit reads different data specific to its functional unit (*Since accessing the NodeId requires accessing a local memory address, the particular processor/memory pair will have to obtain the real address (pointer) to the memory location containing the NodeId data. Since all of the node software executed is located on different processor/memory pairs but are*

Art Unit: 2194

*otherwise identical, the virtual addresses that the programs use are the same, but the real addresses that they map to on each particular processor/memory pair would be unique to that pair, thereby meeting the claim limitation)*

9. As to **Claim 13**, Dunn further teaches wherein the executable program further comprises allocating memory from RAM within the functional unit (pg. 1, para. 3 and pg. 3, source code example) *(The local variables "data[]" and "id" are allocated within the same processor/memory pair, thereby meeting the claim limitation).*

10. As to **Claim 14**, Dunn further teaches wherein the executable further comprises scheduling a program to execute on the processor in the functional unit (pg. 3, para. 2 and pg. 3, source code example) *(When a node does not have sufficient privileges to access a shared memory location, its execution is blocked by a fault until the node that owns that particular location gives it access. The halting and resuming of execution in this manner is a form of scheduling, thereby meeting the claim limitation).*

### ***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Dunn in view of Hubis (US PGPub: 2005/0050191).

13. Dunn discloses the system of **Claim 1**, but does not explicitly teach detecting the Input/Output devices attached to the first functional unit.

14. Hubis teaches automatically detecting devices that have been attached to a system (para. [0045]).

15. One of ordinary skill in the art at the time of invention would have modified the teachings of Dunn with the teachings of Hubis. One would have been motivated by the greater fault tolerance one could achieve by tracking what devices are available in the system and ensuring that all devices that should be available on the system are detected (Hubis: [0045]).

16. **Claims 2, 6-11, and 15-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunn in view of Suzuki (US Pat: 6,092,157).

17. As to **Claim 2**, Dunn discloses the method of **Claim 1**, and further discloses replicating a portion of an operating system into a portion of RAM for both functional units (*[pg. 1, para. 3 and pg. 6, Figure 4] (Each node has a copy of the Linux operating system loaded into memory, thereby meeting the claim limitation)*).

18. Dunn does not explicitly teach the copying of said operating system portion or the attribute information to a read-only portion of RAM.

19. Suzuki explicitly teaches the use of read-only portions of RAM to store program code (*Column 5, Lines 52-62*). Since an operating system is also a program, it would



have been obvious to one of ordinary skill in the art that said operating system code and attribute can be stored in this read-only area. One would have been motivated to do so to ensure that those areas which no longer needed to be modified after system initialization could not be modified (Suzuki: Col. 5, line 52 – Col 6, line 35). Doing so would allow for greater system stability in that executing programs which were not executing properly would be prevented from interfering with critical data. Since, once the system has been initialized, there is no need to modify certain portions, such as the particular program code of the operating system or the NodeId of the node, those areas are ideally suited to be protected in this manner.

20. As to **Claims 6 and 7**, these claims are rejected for the same rationale as provided for the methods of **Claims 1 and 2**, above.

21. As to **Claims 8 and 9**, these claims are rejected for the same rationale as provided for **Claims 3 and 6**, above.

22. As to **Claim 10**, Dunn further teaches wherein each replicated operating system program, when executed by the processors in its RAD, uses the RAS identifier to determine a local RAM for memory allocation (*pg. 3, source code example*) (*The array of shared data is created by the "boss node" by first determining if the node is the boss node ("if (id ==0)" ) and then allocating the necessary array of data locally ("data = new*

*int[3000] ") before sharing that data with the other nodes ("JaDiSM.exportObject("Data", data) ")*

23. As to **Claim 11**, this claim is rejected for the same rationale as provided for **Claims 9 and 14**, above.

24. As to **Claims 15-20**, these claims are rejected for the same rationale as provided for **Claims 6-11**, above.

#### ***Response to Arguments***

25. Applicant's arguments with respect to **Claims 1-20** have been considered but are moot in view of the new ground(s) of rejection.

#### ***Conclusion***

26. Examiner has cited particular columns and line numbers and/or figures in the references as applied to the claims for the convenience of the applicant. Applicant is respectfully reminded that rejections are based on references as a whole and not just the cited passages. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is Applicant's responsibility to read and understand the reference, as a whole, before preparing a reply to this Office Action. Therefore, it is respectfully requested from Applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed

Art Unit: 2194

invention, as well as the context of the passage as taught by the cited art or disclosed by the examiner.

27. The prior art made of record on the P.T.O. 892 that has not relied upon is considered pertinent to applicant's disclosure. Careful consideration of the cited art is required prior to responding to this Office Action, see 37 C.F.R. 1.111(c).

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Pantoliano Jr whose telephone number is (571) 270-1049 and whose direct fax number is (571) 270-2049. The examiner can normally be reached on Monday-Thursday, 8am - 4 pm EST. Please note that a request for an interview in regard to the present application should be accompanied by a written agenda (including proposed amendments, if available, and specific issues to be discussed) sent to the fax number cited above.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Thomson can be reached on (571)272-3718. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2194

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RP  
12/20/2007

  
WILLIAM THOMSON  
SUPERVISORY PATENT EXAMINER